CLAIMS:

1. Electrical circuit arrangement (A) for a display device (6), the electrical circuit arrangement (A) comprising an input terminal (11;13) for receiving a first signal (I_{prog};I_{dat}); a first memory element (M1) for storing information about the first signal (I_{prog};I_{dat}); a driver element (D) coupled to the first memory element (M1) for outputting a second signal (I_{light};I_{prog}) via an output terminal (15;11) in accordance with the information about the first signal; and a calibration circuit (S) coupled between the driver element (D) and the input terminal (11;13) for matching a potential difference between the driver element (D) and the input terminal (11;13) during a calibration phase prior to receiving the first signal (I_{prog};I_{dat}).

2. Electrical circuit arrangement (A) according to claim 1, the calibration circuit (S) comprising a calibration switch (S_{cal}) for coupling the input terminal (11;13) to a calibration voltage (V_{cal}).

3. Electrical circuit arrangement (A) according to claim 1, the calibration circuit (S) comprising a calibration transistor (T_{cal}) coupled with its main terminals between the input terminal (11;13) and the driver element (D); and a second memory element (C_{cal}) coupled to a gate of the calibration transistor (T_{cal}).

4. Electrical circuit arrangement (A) according to claim 3, the calibration circuit (S) further comprising a switch (S5) coupled between one of the main terminals and the gate of the calibration transistor (T_{cal}).

5. Electrical circuit arrangement (A) according to claim 1, comprising a further switch (S3) coupled between the driver element (D) and the output terminal (15;11).

6. Electrical circuit arrangement (A) according to claim 1, comprising a switch (S1) coupled between the driver element (D) and the calibration circuit (S).

7. Electrical circuit arrangement (A) according to claim 1, wherein said driver element (D) is a drive transistor (T2) having a gate connected to said first memory element (M1), and a main terminal coupled to the calibration circuit (S), said gate further being coupled via a switch (S4) to the main terminal of the drive transistor (T2).

8. Electrical circuit arrangement (A) according to claim 1, wherein said first memory element (M1) comprises a capacitor (C)

9. Display device (6) comprising a plurality of display pixels (3), the display pixels (3) comprising an electrical circuit arrangement (A) according to claim 1, and an emissive element (14) coupled to said output terminal (15) and adapted to emit light on reception of said second signal (I_{light}); and a display controller (7) adapted to control the calibration phase of the plurality of display pixels (3).

10. Display device (6) according to claim 9, comprising for each input terminal (11;13) one common calibration switch (S_{cal}) for coupling the input terminal (11;13) to a calibration voltage (V_{cal}).

11. A product comprising the display device (6) as claimed in claim 10; and signal-processing circuitry (SP) for supplying an input signal to a data input (10) of the display controller (7).

12. Column driver (9) comprising a plurality of electrical circuit arrangements (A) according to claim 1, each of said arrangements being adapted to receive a data signal (I_{dat}) as said first signal and to output said second signal (I_{prog}) to a column electrode (11) coupled to a plurality of display pixels (3) along said column electrode.

13. Method for addressing a display pixel (3) of a display device (6) comprising an input terminal (11), a first memory element (C), a driver transistor (T2) coupled to an output terminal (15), and a calibration circuit (S) coupled between the driver transistor (T2) and the input terminal (11), the method comprising the steps of:

- storing information about a first signal (I_{prog}) in said first memory element (C);

- generating a second signal (I_{light}) from said driver transistor (T2) in accordance with the information about the first signal (I_{prog});

- enabling the calibration circuit (S) to match a potential difference between the driver transistor (T2) and the input terminal (11) during a calibration phase prior to receiving the first signal (I_{prog}).